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ЭЛЕКТРОНИКА
И РАДИОТЕХНИКА

EXPERIMENTAL RESULTS FOR LOW-JITTER WIDE-BAND DUAL CASCADED PHASE LOCKED LOOP SYSTEM

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Jitter is a matter of great concern for high-speed digital designers because of its ability to degrade the overall system performance. Designing a low-jitter and wide-band phase locked loop (PLL) system is of practical importance because of its application in high speed digital systems. This paper presents experimental results of a low-jitter wide-band dual cascaded PLL system using a single crystal oscillator. The first PLL employs a voltage-controlled crystal oscillator (VCXO) to eliminate the input jitter whereas the second PLL provides wide bandwidth. Field Programmable Gate Array (FPGA) is used to generate a jittered clock source which is then passed through the proposed system to achieve wide-band and low-jitter signal. Experimental results are presented to validate the proposed technique for different carrier frequencies.

1. INTRODUCTION

Phase locked loop (PLL) is a negative feedback loop basically used to synchronize an output signal with a reference or input signal in phase as well as frequency [1]. A basic PLL consists of three main blocks, namely, the phase detector, the loop filter and the voltage controlled oscillator (VCO). PLL is designed to simplify different tasks such as clock recovery, data retiming, frequency translation and clock smoothing applications. The output signal from the PLL suffers from an associated jitter [2–5] especially at high bit rate resulting in elevated bit error rate (BER) at the receiver side which may cause serious malfunctioning of the overall system if this error exceeds a certain threshold level.

Jitter is defined as the misalignment of edges in a sequence of data bits from their ideal positions and it can cause data errors. Three main types of jitter are cycle-to-cycle jitter [6], period jitter [7] and long-term jitter [8]. As the recovered signal is always jittered it is important to pass the signal through a special circuit to achieve a jitter free or low-jitter signal.

The objective of this paper is to experimentally investigate a low-jitter and wide-band system using two PLLs in cascade configuration. Behavioral modeling and simulation of the proposed system has already been dealt with in a previous paper [9]. Two PLLs as compared to single PLL are capable of operating over a wide frequency range meeting all the requirements of the individual standards in telephone carrier system.

The remainder of this paper is organized as follows. Section 2 presents a brief review of jitter reduction techniques. The details of dual cascaded PLL model is discussed briefly in section 3. Section 4 presents the experimental setup of the proposed system. Experimental results are further discussed in section 5. Finally, conclusions are presented in section 6.

2. JITTER REDUCTION TECHNIQUES

In order to reduce the jitter, it is important to identify the root cause. Many jitter reduction techniques have been reported in the open literature. One of these techniques is to change the filter design to narrow down the PLL bandwidth and to make the phase noise at the VCO input as low as possible [10, 11]. Another technique is to reduce the power supply noise [12, 13]. Heydari et al. proposed a mathematical model for calculating the power supply noise inducing timing jitter in PLLs. This is done by eliminating ground bounce, using additional filter to minimize the effect of the sudden changes of the supply voltage and by having a good grounding to discharge the unexpected charges to ground [13].

A technique proposed for high frequency is by using dual phase frequency detector [14]. This design uses two phase detectors, the first phase detector is a multiplier and the second one is a phase and frequency detector. In [15], a modified low power consumption charge pump is used as phase frequency detector, which proved useful in improving the jitter characteristics of a PLL by blocking the control voltage leakages.

Finally, using a PLL with voltage controlled crystal oscillator (VCXO) helped in generating a stable, low-jitter clock in the recovered signal [16]. A drawback of such technique is that one has to use a VCXO with the same frequency of the input jittered clock. This means that each carrier system needs to use a VCXO working at the same clock frequency. For example, for E_1 tele-

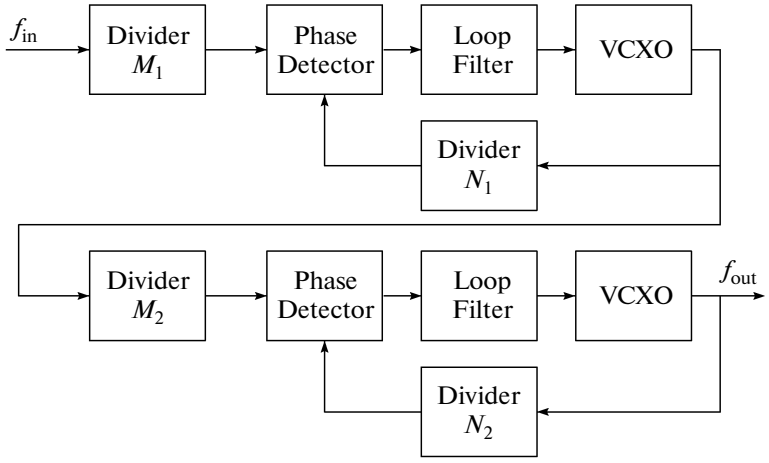

Fig. 1. Dual cascaded PLL system.

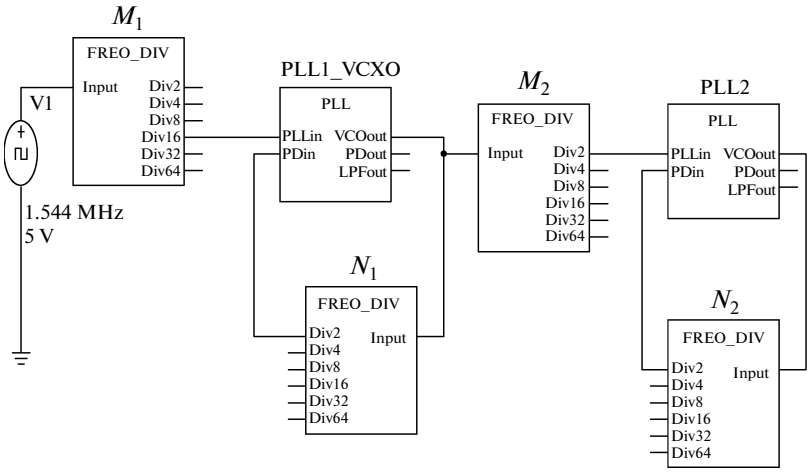

Fig. 2. Circuit Model.

phone carrier system, VCXO has to provide exactly 2.048 MHz signal.

3. DUAL CASCADED PLL SYSTEM

The two important solutions usually used for reducing jitter are those given in [11, 16]. Both these techniques work properly and were successful in reducing the jitter appreciably especially the second one is more effective. Both these techniques may be used for only one bit rate or clock frequency.

For example, in the second technique, a separate VCXO is needed for each bit rate. However, in this paper, we present dual cascaded PLLs as shown in Fig. 1. The recovered clock from the first loop is jitter bounded due to the effect of the VCXO. The second loop is a wide frequency band (wide lock-in range) to cover several standard data rates.

Under steady state operation and while the two loops are in locking conditions, we can deduce the following relationship:

$$f_{out} = \frac{N_1 N_2}{M_1 M_2} f_{in}.$$

The above relationship shows that the output frequency f_{out} may be programmed by selecting (N_1, N_2, M_1 and M_2) to be equal to f_{in}, independent of VCXO frequency when $N_1N_2 = M_1M_2$. It means that we can generate several clock frequencies using single VCXO. The system presented in Fig. 1 is tested experimentally. The details of the experimental setup and the results obtained are presented in the following sections.

4. EXPERIMENTAL SETUP

In order to validate the proposed system we first built a circuit model as shown in Fig. 2. It consists of four dividers (M_1, N_1, M_2 and N_2) and two PLLs. The first one

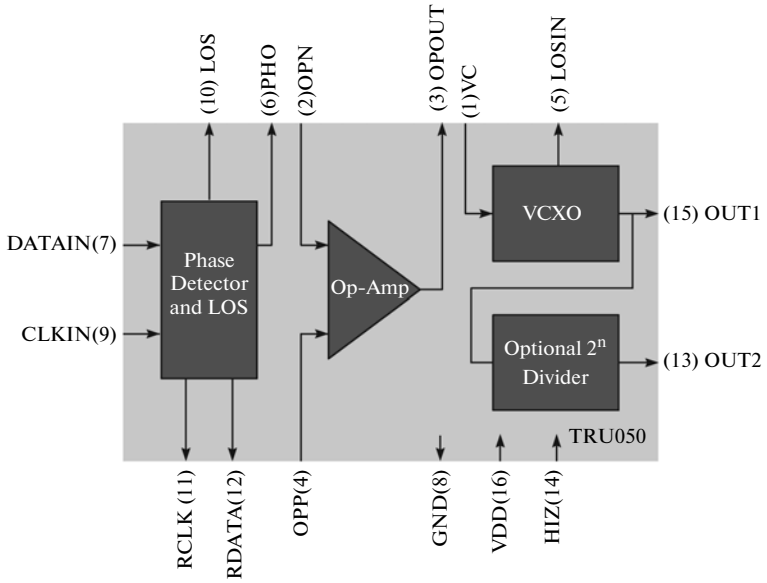

Fig. 3. Block diagram of TRU050 VCXO based PLL.

is a narrow band PLL with a VCXO (TRU050) available from the Vectron international [17]. The block diagram of TRU050 is shown in Fig. 3. The second one is a wide-band PLL with a VCO (74HC/HCT4046) available from NXP semiconductors [18]. It consists of all parts necessary to make a PLL except for the loop filter components. The programmable frequency dividers needed to complete the dual loop structure are built using Xilinx Spartan XCS10 FPGA (Field Programmable Gate Array).

A major problem in this work was to generate a jittered signal for testing because it is difficult to find an appropriate hardware source that can generate such signal. The problem was overcome by using an FPGA test card which is used for checking LeCroy oscilloscopes (WaveRunner 6100 series). This card can generate various jittered signals that can be used for testing the proposed system. Lecroy's jitter and timing analysis (JTA2) software package is used for the measurement and analysis of jitter.

A jittered signal generated using the FPGA test card is fed as an input to the first PLL. A low jittered signal is available at the output. This signal is then fed as an input to the second PLL that is connected in cascade with the first system. The output available from the second system can cover a wide range of frequencies up to 14 MHz.

However, using another PLL with a wider VCO frequency range such as ADF4001 from Analog Devices, it is possible to cover variety of carrier frequencies ranging from T_1 (1.544 MHz) to T_3 (45 MHz) and E_1 (2.048 MHz) to E_4 (140 MHz) [19].

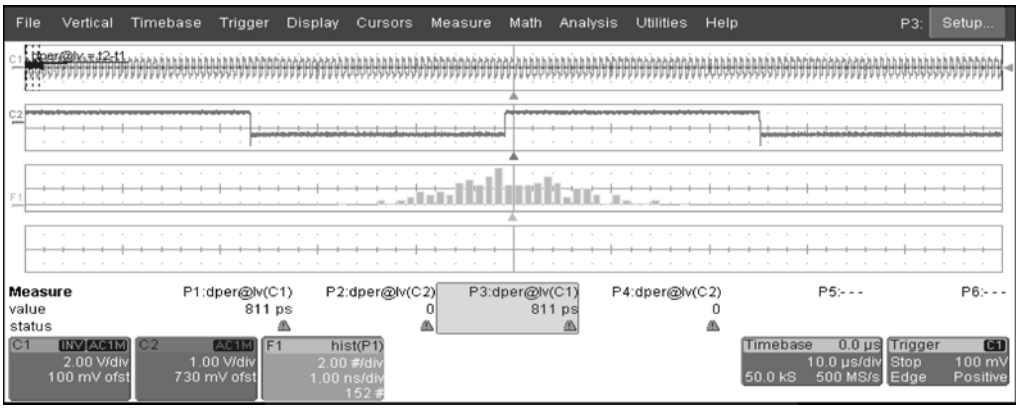

Fig. 4. Jitter measurement for frequency divider ($N = 100$).

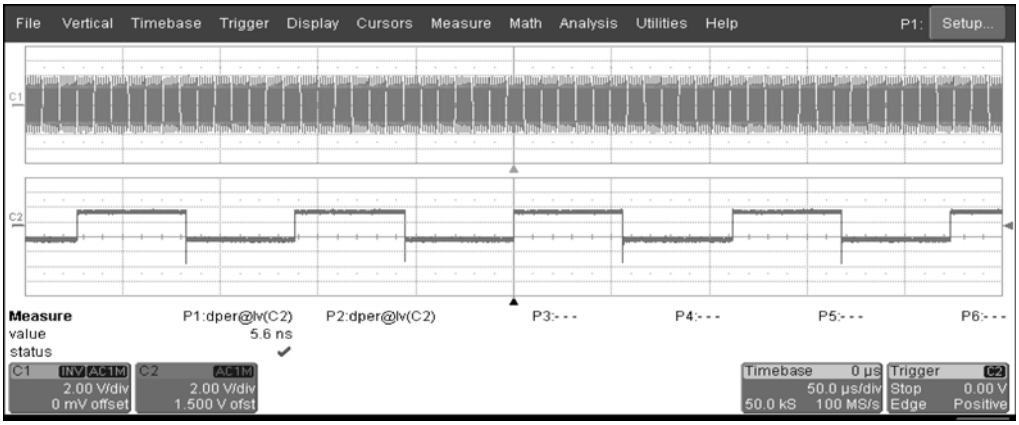

Fig. 5. Jitter measurement for frequency divider ($N = 200$).

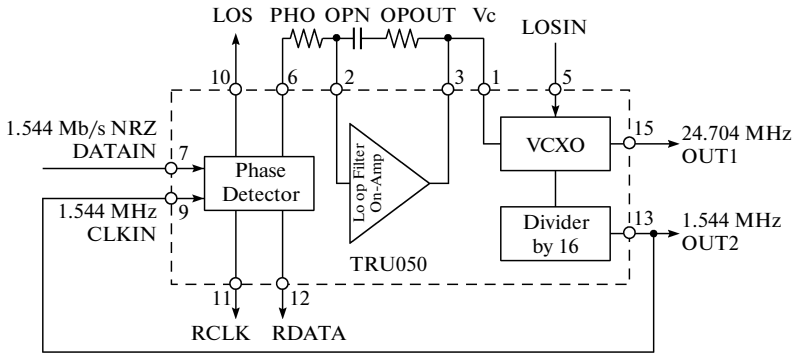

Fig. 6. Configuration of first PLL (TRU050) [17].

5. EXPERIMENTAL RESULTS

Four types of measurement were done to measure:

1) Cycle-to-cycle jitter;

2) Root mean square (RMS) jitter;

3) Accumulated jitter;

4) Time interval error (TIE).

The four frequency dividers were built using a 74192 counter plus a D-Type flip-flop to cover wide range of frequencies and 50% duty cycle respectively.

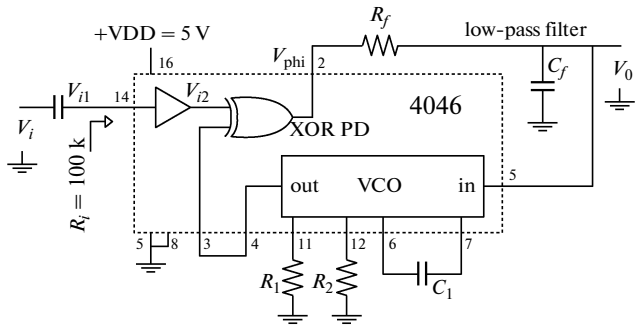

Fig. 7. Configuration of second PLL (74HC4046) [18].

We also used Xilinx Spartan XCS10 FPGA based board to modify the value of the dividers. Figure 4 depicts the output signal of the frequency divider with $N = 100$, measured using a high-speed oscilloscope. The measured jitter in this case is 811 ps as shown in Fig. 4. For a divider with $N = 200$, the measured jitter is 5.6 ns as shown in Fig. 5. Jitter in both the cases is reduced after passing through the frequency dividers.

The first PLL circuit was implemented with external components that include resistors and capacitor. The circuit diagram is shown in Fig. 6. The second PLL (74HC4046) contains all the necessary parts to implement a PLL except for a handful of resistors and capacitors. Resistor of values 10, 20 and 330 kΩ as well as capacitors of capacitances 0.1 and 2.2 µF are used. The circuit diagram of the second PLL is shown in Fig. 7.

By applying highly jittered signal to the system and measuring the output jitter at frequency 1.544 MHz (T_1 Carrier), we can deduce the jitter behavior of the system. The output from the oscilloscope is as shown in Fig. 8, where the upper part represents the carrier frequency. The middle portion of the figure shows the tracking jitter. The lower portion is the jitter histogram. The jitter statistics considered in this paper are

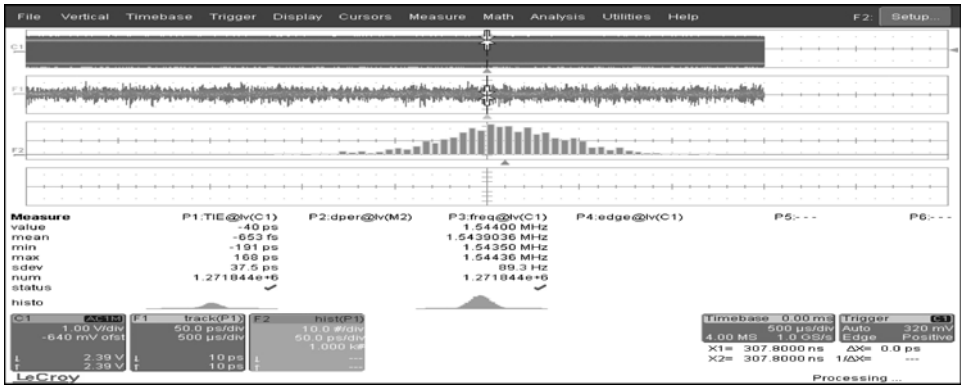

Fig. 8. Jitter measurement for T_1 carrier (1.544 MHz).

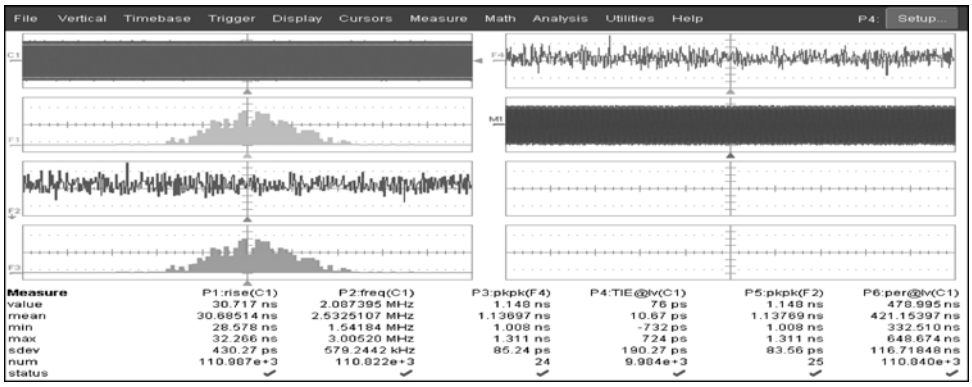

Fig. 9. Jitter measurement for E_1 carrier (2.048 MHz).

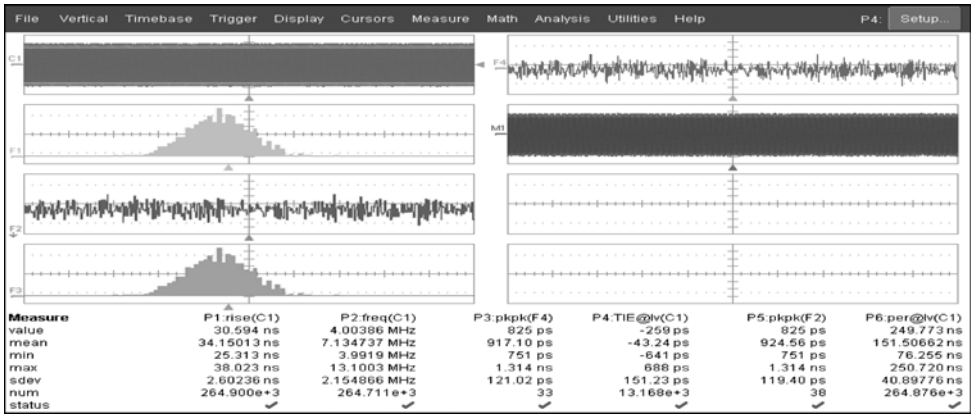

Fig. 10. Jitter measurement for 4 MHz carrier.

cycle to cycle jitter, RMS jitter and accumulated jitter. The TIE has also been measured. TIE measures the position of each edge in a waveform and compares it to the position the edge would have if the waveform frequency was perfect. This analysis can reveal modulation effect, phase noise, and other sources of timing variations. As shown in Fig. 8, the output jitter is reduced to 37.5 ps as compared to the input jitter which is 5.6 ns.

The same experimentation is done for E_1 carrier (2.048 MHz). As can be seen on the left hand side of Fig. 9, the carrier frequency (E_1), its histogram, track-

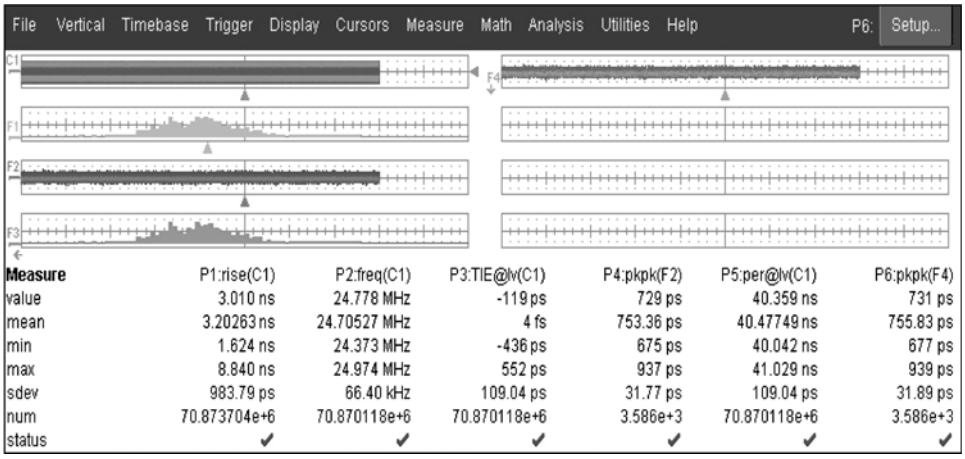

Fig. 11. Jitter measurement for 24.77 MHz carrier.

ing jitter and the jitter histogram are represented from top to bottom. The right hand side of the Figure from top to bottom shows another reading of the tracking jitter and the restored carrier frequency respectively. The same jitter statistics are considered here. As shown in Fig. 9, the value of the jitter was reduced from 5.6 ns in input to 85 ps in the output.

The process of jitter measurement was repeated for different values of carrier frequency such as 4 MHz (Fig. 10), 13 MHz and 24.77 MHz (Fig. 11). The input and output jitters for different carrier frequencies are summarized in Table.

6. CONCLUSIONS

PLL is an important module used in mixed signal integrated circuits and systems. It is widely used for clock recovery, data retiming, frequency translation and clock smoothing applications. However, jitter in PLL causes set-up and hold-time violations in digital circuits and this leads to data transmission errors. Hence, it is necessary to use jitter-free or low jitter signal source.

In this paper, a low-jitter and wide band dual cascaded PLL system is experimentally verified for different carrier systems such as American ($T_1 - T_3$) and European ($E_1 - E_4$). The recovered clock from the first PLL is jitter bounded due to the effect of the VCXO. The second PLL is a wide frequency band (wide lock-in range) to cover several standard data rates.

The experimental results demonstrate that the jitter behavior is almost directly proportional to the carrier frequencies ranging from 1.54 MHz up to almost 10 MHz, and then it remains almost constant for frequencies ranging from 10 MHz up to 24.77 MHz. Lecroy's JTA2 software package is used for the advanced jitter and timing analysis. The experimental result verifies the validity of the proposed system.

Jitter measurement summary

Carrier frequency, MHz	Input Jitter, ns	Output Jitter, ps
1.544 (T_1)	5.6	37.5
2.048 (E_1)	5.6	85
4	5.6	121
13	5.6	160
24.77	5.6	109

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