ПРИБОРЫ И ТЕХНИКА ЭКСПЕРИМЕНТА, 2011, № 2, с. 32–38

ПРИМЕНЕНИЕ ВЫЧИСЛИТЕЛЬНОЙ ТЕХНИКИ В ЭКСПЕРИМЕНТЕ

A TIME TICK BASED METHOD FOR MEASURING STATIC ERRORS OF ADC

© 2011 K. Hariharan, R. K. M. Rajkumar, V. Abhaikumar

Thiagarajar College of Engineering, Madurai Tamilnadu, India

Received August 23, 2010

This paper presents a novel Time Tick based Built In Self Test (TT BIST) for measuring the static errors of an Analog to Digital Converter (ADC). The proposed method determines the period elapsed during transition between two consecutive digital levels and compares it with the ideal period of transition. A counter that works, at higher speed relative to the sampling rate of the ADC under test, is used. It counts the number of time ticks occurred during every transition. The required ramp signal is generated dynamically, using current source with digital switch for selecting the equivalent test signal. Further to support testing of errors in ratiometric ADC, a slope conditioning module is also implemented. The entire computation cycle is done in a single ramp cycle whereas in conventional histogram method multiple waveforms are required. Thus, the proposed TT method requires less time to achieve desired accuracy levels by choosing the appropriate slope of the ramp signal.

INTRODUCTION

The full test of an Analog-to-Digital Converter (ADC) involves the determination of two kinds of parameters, the static errors linked to some deviations of the converter transfer function, and the dynamic features expressing the distortion and noise of the converted signal introduced by the converter. Further, there are two methods of measurement for an ADC, Single-ended measurement and ratiometric [1] measurement. The difference between the two methods is in the ADC reference voltage. In single-ended mode, the ADC is referenced to ground and to V_{ref} (V_{ref} can be either the internal reference voltage or an external reference). For the ratiometric measurement, the ADC is referenced to the excitation voltage. Ratiometric testing is chosen to avoid error in the testing due to errors in reference voltage.

Measurement of ADC static errors such as Non Linearity errors, Offset error and Gain error is critical in applications requiring matched converters, such as interleaving, simultaneous sampling, and I/O signal processing, where there is a need to match relative gain and offset between individual converters [2]. Static errors are generally deduced from a histogram based test [3] lying on a statistical analysis of the occurrence frequency for each output code while dynamic parameters are usually evaluated from the spectral distribution of the converted signal. In this paper, we seek to provide an alternative to the more costly and longer histogram-based analysis, which requires a very high number of samples to obtain satisfactory statistical results [4, 5].

SYSTEM DESIGN FOR TIME TICK BIST

The proposed TT BIST method is implemented as given in the block diagram in Fig. 1. The Slope Conditioning module can be turned on whenever ratiometric ADC's is to be tested. Exploitation module gets the code for each transition from the ADC under test. It counts the number of ticks for every code transition, until the received code is equal to the pre-loaded code. The measured Time ticks for each code transition are updated to the memory instantaneously.

EXPLOITATION MODULE

In the Exploitation module as shown in Fig. 2, counter *CNT_TT* counts the time-ticks between each digital-code transition induced by the ramp. For this, a reference counter provides the value of the next digital level relative to the ramp's current input to the ADC. This counter is initially set to a value one greater than the ADC's minimum value. The clock to the reference counter is supplied through a loop back from the comparator. The comparator outputs logic high only when C_N is less than D_N.

Thus, when the ADC's equivalent code to the input ramp equals the first count of the reference counter, the counter gets incremented to the second count and the process is repeated until the ramp reaches ADC full-scale code. *CNT_TT* is enabled when C_N is less than D_N and thus provides time ticks between each digital code transition, TT_p (i). A delay-buffer provides minimal delay for the latch to capture each TT_p (i) and then *CNT_TT* is cleared (*CLR*) to count the next TT_p. The output from the comparator is also used as an interrupt to the Processing block.

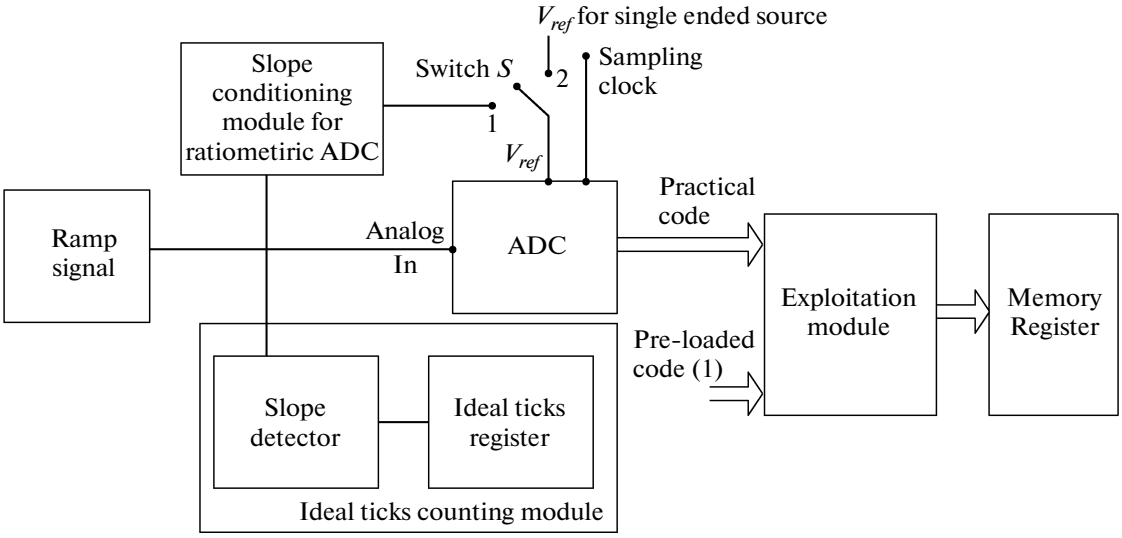

Fig. 1. Block diagram of TT BIST.

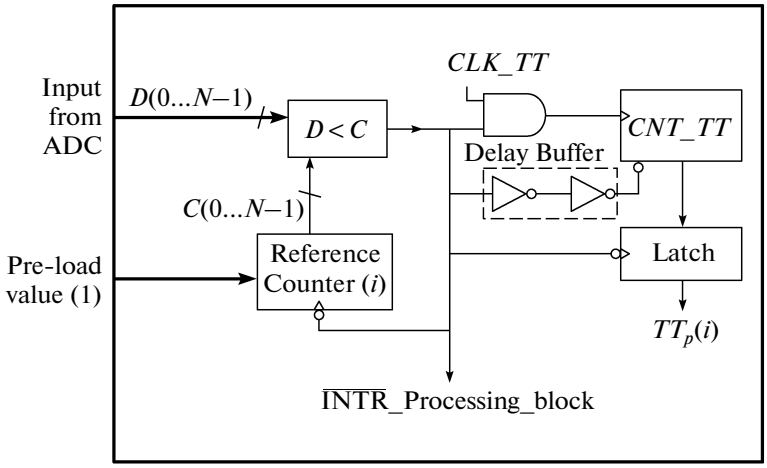

Fig. 2. Exploitation module.

The Preload input (default cases it is 1) provided to the Reference counter can be used to directly calculate the value of any i-th code non-linearity error. If the time taken by a ramp to produce a digital transition in the output of the ADC is ΔT then the frequency of the ramp is maintained such that $\frac{1}{\Delta T} < \frac{CLK\_TT}{N}$ where CLK_TT is the pre-scaled frequency from the internal clock of the System On Chip (SOC), supplied as clock to CNT_TT and N is the precision tune factor of the error estimate. Ideally, ΔT is constant for ramp input but varies due to the static errors. If ΔT_{ideal} is the ideal output transition period for the same input in an ideal ADC, then the errors may be found as a function of $T_{ideal} - \Delta T$.

IDEAL TICKS COUNTING MODULE

To estimate the Ideal Time ticks (TT_i) for a Least Significant Bit (LSB) value, it is required to relate the ideal time period to the slope of the input. This is done through a limiting and slope detection circuit as shown in Fig. 3.

The two comparators in the circuit are provided with upper threshold voltage (V_{ut}) and a lower threshold voltage (V_{lt}), where the difference between the threshold voltages is the LSB value. For a ratiometric measurement the thresholds are fixed dynamically based on the reference voltage. The enable clock (EN_C) signal holds a high logic when the ramp is detected in between the thresholds V_{ut} and V_{lt} and the counter CNT_SR obtains the number of ticks taken by the ramp for this period. Thus, TT_i is found as

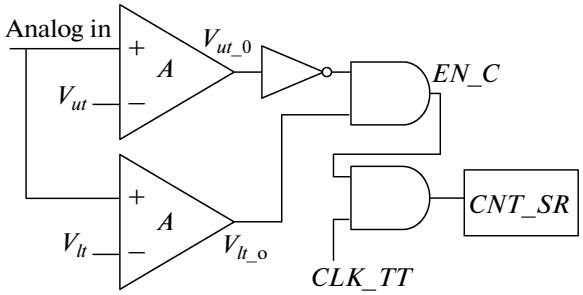

Fig. 3. Slope detection circuit.

$$TT_i = \frac{CNT\_SR_{latch}}{2^n - 1} \times \frac{V_{ref}}{V_{ut} - V_{lt}}. \quad (1)$$

The algorithm for measuring the trace period of ramp signal is as follows. It finds the number of time ticks between every two digital transition (TT_i):

TT_total = 0

Wait until $EN\_C = 1$ // $EN\_C = \overline{V_{ut\_0}}$ & V_{lt_0}

While $EN\_C = 1$

TT_total++

End loop

$TT_i = (TT\_\text{total} \times k)/(2^n - 1)$ // $k = (V_{ref}/(V_{ut} - V_{lt}))$.

ERROR COMPUTATION

If F_s is the ADC sampling frequency and T_r, the ramp signal time period, V_{in} is the input voltage and V_{fs} is its full-scale voltage, then the system design is as follows.

Time period for an Ideal Digital transition T_{ideal}:

$$\Delta T_{ideal} = \frac{V_{\text{LSB}}}{V_{fs}} T_r, \quad (2)$$

where V_{LSB} is the resolution of ADC.

For ratiometric measurements, T_{ideal} is calculated as

$$\Delta T_{ideal} = (V_{fs} - V_{in}) \frac{V_{\text{LSB}}}{V_{fs}} T_r. \quad (3)$$

Hence, the number of time ticks per ideal digital transition is given as

$$TT_i = F_s \Delta T_{ideal}. \quad (4)$$

Let $TT_p(i)$ be the number of time ticks obtained practically for every i-th code transition. Error factor e, can be obtained as

$$e_i = TT_p(i) - TT_i. \quad (5)$$

The e_i value obtained from equation (5) for the first count alone signifies the *offset error*. The values for each count furnish the *DNL error*. When $i > 0$

$$DNL(i) = \frac{TT_p(i) - TT_i}{TT_i}. \quad (6)$$

The *INL error* value for the i-th code transition is also obtained as follows:

$$INL(i) = INL(i - 1) + DNL(i). \quad (7)$$

Pseudo code for calculation of $TT_p(i)$ for all our calculations is given as follows:

```
Ref_counter = 1
TT_counter = 0
Wait until EN_C = 1
ADC_value = getValue_ADC ()
i = 0
While (ADC_value < 2^n−1)
{
    ADC_value = getValue_ADC()
    If Ref_counter > ADC_value then
    TT_counter++
    Else
    {   TT_P (i) = TT_counter
        TT_counter = 0
        Ref_counter++
        i++
    }
} End Loop
```

Gain error can be calculated as the full-scale error minus the offset error. Full-scale error is the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. The number of ticks for the ramp to sweep the Full-scale range in an ideal ADC is given as $TT_{f(ideal)} = TT_i \cdot 2^n$, where n is the number of bits of the ADC. The full-scale error is calculated as

$$e_f = \frac{TT_f - TT_{f(ideal)}}{TT_i}. \quad (8)$$

TT_f is the CNT_SR time tick value for the digital output to reach full-scale for the given input ramp. Gain error may thus be found as

$$G_e = e_f - DNL(1). \quad (9)$$

RAMP SIGNAL GENERATION

Ramp signal generation methods such as Ramp Generators for Mixed-Signal [6], SSLAR ramp signal [7], Low-cost Adaptive Ramp Generator [8], and high precision ramp generator [9] have signals, whose slope depends on passive device. However, we may need

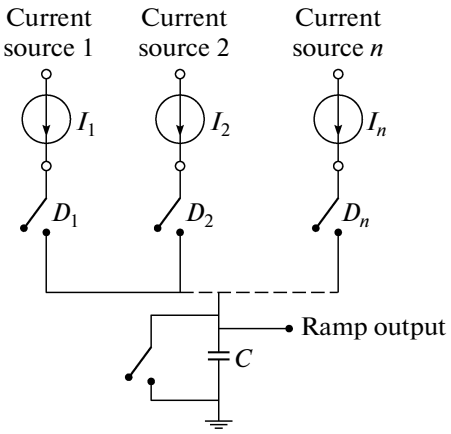

Fig. 4. Digitally switchable Ramp source.

ramp signal with dynamically switchable slopes for ADC testing with varying accuracy.

DIGITALLY SWITCHABLE RAMP SIGNAL

The current sources are digitally controlled providing us different ranges of current, which are used for generation of variable slope ramp signals. Ramp signals generated are of high precision and can be effectively used in ADC static and dynamic error testing. Current can be varied by digitally switching them, as shown in the Fig. 4:

$$I_{final} = \sum_{k=1}^{n} I_k D_k. \tag{10}$$

Assuming $n = 3$, current sources as above with different current values, we can have 7 $(2^n - 1)$ different combinations of resulting current. These current will change the slope accordingly.

RAMP CONDITIONING FOR RATIOMETRIC ADC

In ratiometric [1, 10] ADC test, the rising ramp input signal is given to the analog input of ADC. Simultaneously a falling ramp input signal is given to the reference voltage of the ADC. The sum of these two signals should not exceed the full-scale voltage of the ADC. A triangular wave generator is used, and ramp signal is isolated from it, for the experiment.

The digital output of the ADC is given by

$$D_{out(ideal)} = A\frac{2^n}{V_{ref}}, \tag{11}$$

where $A = V_{in} \pm V_x$ and $-\frac{1}{2}V_{\mathrm{LSB}} \le V_x < \frac{1}{2}V_{\mathrm{LSB}}$, V_x is the normalization voltage to nullify the error due to quantization for the purpose of ideal modeling.

The DC errors of non-ideal ADC are offset voltage error and gain error. The effective D_{out} may be given as

$$D_{out} = (A \pm V_L)\frac{2^n}{V_{ref}(1 - G_e)}. \tag{12}$$

Here, V_L is the linearity error voltage of the ADC and varies for each code value, and is the gain error which is the ratio of gain difference between actual gain and ideal gain to the value of the actual gain.

Ratiometric conversion is done by means of an inverting amplifier and an inverting adder circuitry, thus making the ratio of V_{in} to V_{ref} a linear one. The circuit for the conversion is shown in Fig. 5 and the corresponding waveform is shown in Fig. 6.

RESULTS AND DISCUSSION

MAX162, a 12-bit ADC is used as the device under test. ALTERA DE1 board containing cyclone FPGA is used to implement the proposed circuit and to obtain data from the ADC. The data and control bus of

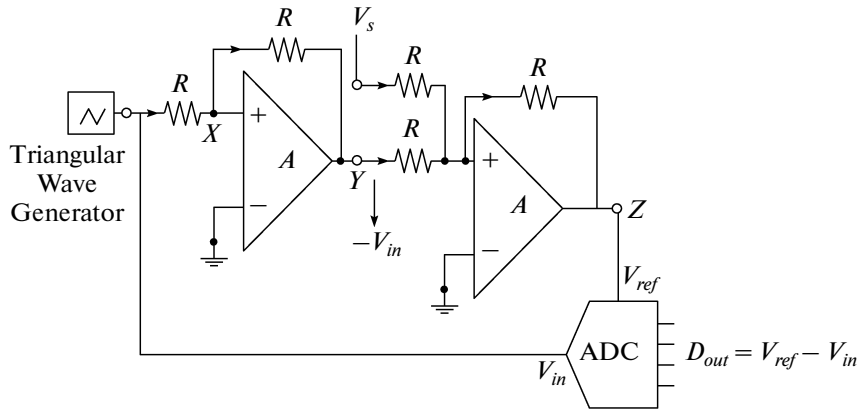

Fig. 5. Ratiometric signal conditioning circuit.

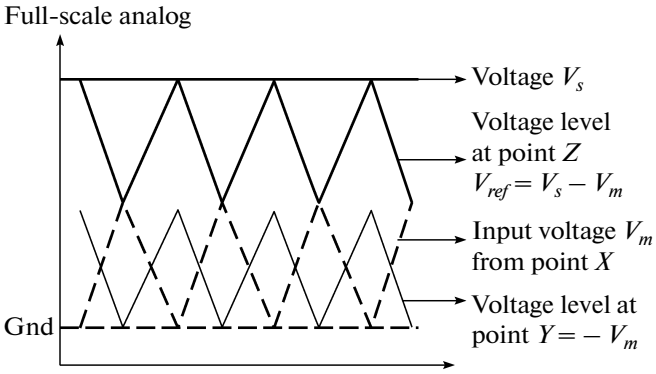

Fig. 6. V_{ref} and V_{in} generated from circuit in Fig. 5.

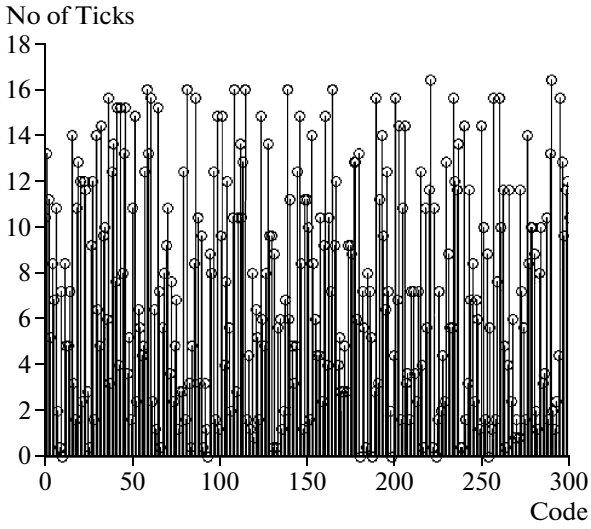

Fig. 7. Time Tick values for MAX162 up to Code 300.

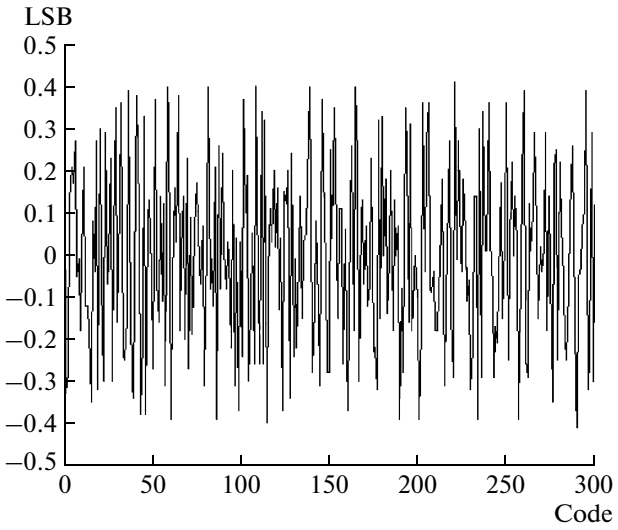

Fig. 8. *DNL* error values for MAX162 up to Code 300.

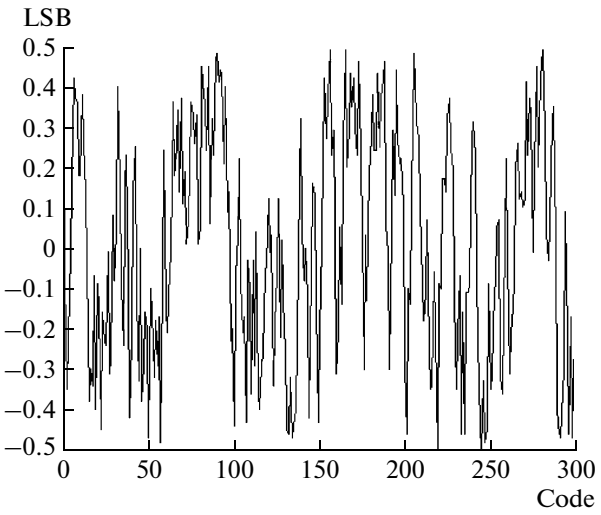

Fig. 9. *INL* error values for MAX162 up to Code 300.

the MAX162 are connected to the FPGA through GPIO pins provided in ALTERA board.

The Conditioned Ramp signal of frequency 1.22 Hz was generated dynamically and was given to Ideal ticks counting module and to ADC under test. The ADC was tested for various input signals, and the corresponding results are tabulated in Table 1.

Table 1. Number of ideal time ticks

Bits of ADC	Sampling frequency, kHz		
	100	200	300
8	160 (ticks)	320 (ticks)	481 (ticks)
10	40 (ticks)	81 (ticks)	120 (ticks)
12	10 (ticks)	20 (ticks)	30 (ticks)

Thus, for the given setup a 12-bit ADC output obtained at a sampling frequency of 200 kHz, with number of time ticks, $TT_i = 20$ ticks for a ΔT_{ideal} value of 0.1 ms, is used for all further calculations. However, due to various static errors, the value of TT_p was found to be varied for each code word. These digital output data were then stored in SDRAM A2V64S40C. Simultaneously the slope of the given ramp was also found out using another counter *CNT_SR* and was used to calculate the TT_i. This calculation is necessary to avoid errors due to minor deviations of the ramp input from the maximum limit V_{ut}. The static errors were

found from the equations (5)–(9). The entire error determination is done in a single ramp cycle.

The errors were calculated using the design formulae and the obtained values, TT_i and TT_p.

For the given input, the value of ΔT_{ideal} is proportional to 20 time ticks. Hence, the resolution is 0.05 LSB (1/20). It can be increased further by increasing the number of time ticks per code word. The errors obtained were compared with the values given in the datasheet of MAX 162 as in Table 2.

The *DNL* error obtained for each digital output was found to be in accordance with values predicted by histogram method. The *DNL* and *INL* errors were obtained from time ticks (TT) value as shown in Fig. 7–Fig. 9 respectively. The method is effective in determination of the errors as proven by comparisons shown in Fig. 10 and Fig. 11.

Implementation on FPGA shows that such a system could be applied to a SOC, hence a compact and accurate BIST system for determination of static errors is achieved. The proposed system may also be extended to calculate dynamic errors.

Further to our earlier discussion, Histogram BIST (H BIST) method needs higher number of computation and hence time consuming, while in TT BIST method the complexity is hugely reduced, because only the number of ticks are determined, rather than number of code occurrences. It is important to note here that, in Histogram method the input signal, often produces an overdrive resulting in higher extreme code occurrences, but a similar situation is averted in TT BIST, because when signal reaches the full scale level, Ticks computing is stopped. Miscalculated errors, as reported in Hybrid BIST are avoided, as TT BIST method avoids the use of any on-chip DAC's. Probability of error is minimized because, the ideal values are not pre-computed values, rather they are dynamically generated every time we pass an input.

Table 2. Comparison of obtained values using TT BIST with values obtained using Histogram method

Static Errors	TT BIST method (in LSB)	Histogram method (in LSB)
Offset Error	+3.5	+3.8
Full-scale Error	+12.85	+12.91
Gain Error	+9.35	+9.42
INL Error	–0.3	–0.3

In [11] Histogram BIST based on time decomposition and space decomposition is discussed, and test time follows the formula

$$T_{test} = 3 \cdot (32/F_s) \cdot 2^n, \quad (13)$$

where F_s is the sampling frequency, n denotes the number of bits under test, 32 is H_{ideal} (Ideal Histogram value). Factor 3 represents three phases of test for offset gain and *NL* errors. In TT BIST all three parameters are observed in single cycle.

The testing time $T_{test\_proposed}$ satisfies the below equation:

$$T_{test\_proposed} = (32/F_s) \cdot 2^n. \quad (14)$$

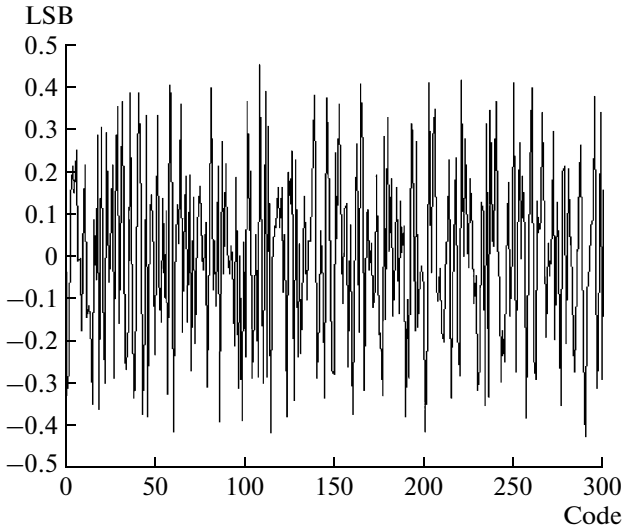

Fig. 10. *DNL* error values estimated by histogram method for MAX162 up to Code 300.

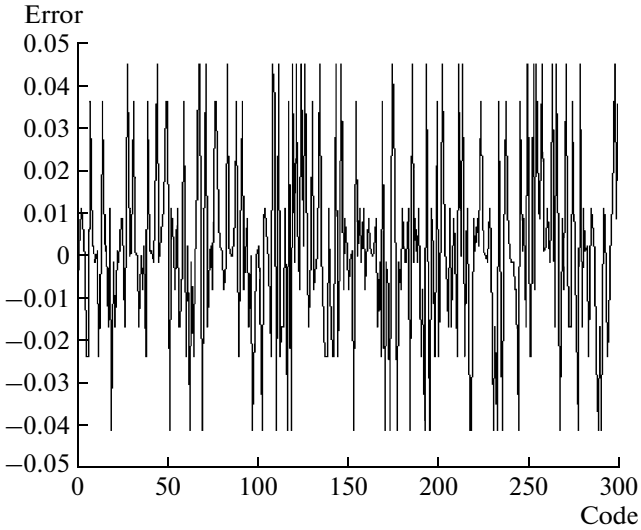

Fig. 11. Error Estimation difference between TT BIST and Histogram method.

CONCLUSION

This paper proposes a time tick based TT BIST method for ADC. This technique utilizes an exploitation module and an ideal ticks counting module, to measure static errors with reduced complexity and testing time. A practical implementation is described and the performance is evaluated. Operational amplifier, an analog component, is used for ratiometric measurements. This can be a source of limitation during 'on chip' testing. But by increasing the gain parameter of the operational amplifier, the dependence of the error on the analog system input (minimum resolvable voltage level) can be made very slight, thus overcoming the limitation. Currently, we are studying the probability of error for the system, for extreme values, to make this technique more effective and universal.

REFERENCES

1. Hariharan, K., Vasanthakumar, P., Varun, G., Abhaikumar, V., *Measurement Science Review*, April 2010, vol. 10, pp. 56–59.
2. Maria da Glória Cataldi Flores, Marcelo Negreiros, Luigi Carro, and Altamiro A. Susin, *IEEE Transactions on Instrumentation and Measurement*, October 2004, vol. 2, pp. 1350–1353.
3. Jianguo Ren, Jianhua Feng, Hongfei Ye, *9th IEEE International Conference on Solid state and Integrated Circuit Technology* (*ICSICT*), October 2008, pp. 2099–2102.
4. Azaies, F., Bernard, S., Bertrand, Y., and Renovell, M., *IEEE European Test Workshop*, Cascais, Portugal, May 2000, pp. 213–224.
5. Dasnurkar, S., Abraham, J.A., *IEEE International Symposium ISCAS*, Taipei, Taiwan, 2009, pp. 9–12.
6. Na Zhang, Suying Yao, and Yu Zhang, *Springer Journal on Transactions of Tianjin University Solid-State-Circuits*, February 2003, vol. 38, pp. 178–181.
7. Sakkarapani Balagopal, Suat U. Ay, *52nd IEEE International Midwest Symposium on Circuits and Systems*, Cancun, Mexico, August 2–5, 2009, pp. 373–376.
8. Azaïs, F., Bernard, S., Bertrand, Y. et al. *19th IEEE Proc., VLSI Test Symposium*, April 2001, pp. 266–271.
9. Wen-Ta Lee, Yi-Zhen Liao, Jia-Chang Hsu, et al. *9th IEEE International Conference on Solid state and Integrated Circuit Technology* (*ICSICT*), October 2008, pp. 2103–2106.
10. Russell Anderson, *Texas Instruments Application Report SBAA110* – March 2004.
11. Jianguo Ren, Teng Lin, Jianbing Zhao, et al. *Verigy integrated circuit testing techniques conference*, China, November 6, 2007, pp. 1498–1507.